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EXAMINER

EDMONDSON, LYNNE RENEE

| ART UNIT | PAPER NUMBER |
|---|---|
| 1725 | // |

DATE MAILED: 04/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

H-C

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/868,573 | ZEN, MITSUO | |
| | Examin r | Art Unit | |
| | Lynne Edmondson | 1725 | |

*-- The MAILING DATE of this communication app ars on the cover she t with th correspond nce address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *16-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 16-23, 25, 27, 28, 30, 34 and 39 are rejected under 35 U.S.C. 102(a) as being anticipated by McAndrew (USPN 6095404).

McAndrew teaches a method of forming a solder coated material comprising the steps of electroplating a layer of material having excellent solderability such as Ni or Au containing layers having a thickness of 1.27 to 5.5 microns (50 microinches to 220 microinches, col 2 lines 1-15) on a substrate comprising Fe-Ni (col 4 lines 53-59) and then passing the difficult to solder material through molten solder to form a dip solder plating layer having a thickness of about 13 microns (500 microinches) (col 4 lines 20-32) by wave soldering (col 4 line 35). The solderable material may be a Sn-Ag alloy (col 2 lines 30-38). Although electroplating and hot dipping are taught in the method, an

identical structure can be formed by screen printing the layers. See also McAndrew claims 1 and 5-9.

2. Claims 16, 18-20, 22, 23, 25, 26, 28-30, 34, 39 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Tadauchi et al. (USPN 6123248).

Tadauchi teaches a method of forming a portion to be soldered comprising the steps of electroplating (flash plating) a layer of material having excellent solderability (gold) on a substrate comprising Ni wherein the plated layer is 0.5 microns (col 17 lines 1-22) and the solder layer is about 15 microns (col 16 lines 18-22 and col 17 lines 25-27) typically between 5 and 50 microns (col 12 lines 63-65). The molten solder is dip coated via ultrasonic wave soldering (col 16 lines 9-18) in an inert atmosphere (col 7 lines 37-39 and col 9 line 58 - col 10 line 41). The solder is a Sn-Ag alloy (col 4 line 65 and col 17 lines 30-55). It is noted that the structure, the portion to be soldered can have the same structure if the plated layers are applied by different means such as screen printing. See also Tadauchi claims 1, 2, 4, 8 and 9.

3. Claims 16, 18, 20, 22, 25, 28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Siemens AG (DT 2340423 A).

Siemens teaches a method of forming a solder coated material comprising the steps of electroplating a layer of material having excellent solderability such as Ni or Cu having a thickness of 1 micron on a substrate comprising and then passing the difficult to solder material through molten solder to form a dip solder plating layer having a

thickness of about 50 microns (abstract). Although electroplating and hot dipping are taught in the method, an identical structure can be formed by screen printing or vapor deposition of the layers.

4. Claims 16, 18-20, 22, 23, 31, 34, 35, 39 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Izuta et al. (USPN 5609287).

Izuta teaches a method of forming a solder coated material comprising the steps of electroplating a layer (second solder 5b) of material having excellent solderability such as solder having a thickness of 1 micron (figure 1 and col 2 lines 53-55, col 7 lines 51-54 and col 12 lines 55-60) on a substrate and then forming a second layer (first solder 4) having a thickness of 50 microns (col 2 lines 48-57, col 3 lines 10-18 and col 7 lines 8-15). The solderable material may be a Sn-Ag alloy (col 13 lines 1-7). An identical structure can be formed in a variety of ways including but not limited to dipping, screen printing, CVD and electroplating. The substrate may be a lead frame (col 1 lines 20-25). See also Izuta claims 1-19.

5. Claims 16-24, 31, 43 and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyahara (USPN 5629559).

Miyahara teaches a method of forming a solder coated material such as a package lid (cap) or lead frame (col 1 lines 1-12 and lines 39-55) comprising the steps of electroplating a layer of material having excellent solderability such as Ni, Cu or Au (col 7 lines 13-40) having a thickness of 2 microns (col 15 lines 45-65) on a substrate

comprising Fe-Ni (col 7 lines 41-47) and then forming a solder layer having a thickness of 40 microns (col 15 lines 27-31). The solder or solderable material may be a Sn-Ag alloy (col 8 lines 51-67). An identical structure can be formed in a variety of ways including but not limited to dipping, screen printing, CVD and electroplating.

6. Claims 16, 18, 20, 22, 25, 28, 34, 39 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohno (USPN 4666078).

Ohno teaches a method of forming a solder coated material comprising the steps of electroplating a layer of material having excellent solderability such as Ni or Cu (col 2 lines 5-23 having a thickness of 5 microns (col 4 lines 29-37) on a substrate and then passing the difficult to solder material through molten solder (bath) to form a dip solder plating layer having a thickness between 0.1 and 300 microns (col 4 lines 38-63 and col 5 lines 20-61). Although electroplating and hot dipping are taught in the method, an identical structure can be formed by screen printing or vapor deposition of the layers. See also Ohno claims 3-7, 11-16 and 19-22.

7. Claims 16, 18, 20, 22, 25, 28, 30, 34, 39 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Powell et al. (USPN 6160310).

Powell teaches a method of forming a solder coated material comprising the steps of electroplating a layer of material having excellent solderability such as Ni or Au to a thickness of 2 to 12 microns (col 5 lines 18-25) on a substrate and plating a 25 micron thick layer of solder to the plated layer (col 5 lines 15-25). Although the method

of depositing the layers does not change the structure, it is noted that the thin layer may be formed by electroplating (col 2 lines 51-53) and a dip solder plating layer may be formed by wave soldering (col 8 lines 10-25). The method is used to join surface mounted connectors (col 1 lines 13-29 and figures 3-5). See also Powell claims 7 and 10.

8. Claims 16-18, 20-22, 24, 25, 27, 28, 31, 34, 36, 39, 41, 42, 44, 46 and 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Geschwind (USPN 4331258).

Geschwind teaches a method of bonding a lid to a package or lead frame (col 2 lines 53-64 and col 3 lines 1-12) comprising the steps of electroplating a layer of material having excellent solderability (gold or nickel) on a substrate comprising Fe-Ni (col 1 lines 25-32 and col 4 lines 12-27) wherein the plated layer is 1.2 to 2.5 microns and the solder layer is 50 microns (2 mils, col 2 lines 35-52). The molten solder is coated by dipping (col 4 lines 32-66). See also Geschwind claims 1-7.

9. Claims 16-18, 20-22, 24, 31, 34 and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagashima et al. (USPN RE34484).

Nagashima teaches a method of forming a solder coated material comprising the steps of electroplating a layer of material having excellent solderability (gold) on a substrate comprising Fe-Ni (Kovar) (col 5 lines 1-6 and col 4 lines 16-33) wherein the plating thickness is 0.5 to 5 microns (col 2 lines 15-47 and col 3 lines 3-27) and then passing the difficult to solder material through molten solder to form a dip solder plating

layer (col 4 lines 30-33). The solder has a thickness of about 50 microns (col 4 lines 17-20) The method may be used to join a lid of a packaged part, lead (col 4 lines 16-33) or a connector (col 2 lines 5-14) and may be performed in an inert atmosphere (col 4 lines 5-19). See also Nagashima claims 1 and 2.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 25, 27, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherry (USPN 4763829) in view of Svendsen et al. (USPN 5262718).

Sherry teaches a method of forming a solder coated material comprising the steps of forming a layer of material having excellent solderability such as Ni or Au to a thickness of 1.2 microns (col 2 lines 6-15 and col 4 lines 5-18) on a substrate and plating a 25 to 35 micron thick layer of solder to the thin layer (col 3 lines 45-56 and col 4 lines 5-18). The solder is applied by ultrasonic wave soldering (col 1 lines 47-57 and col 2 line 56 – col 3 line 25). However, there is no disclosure of the method of forming the thin layer.

Svendsen teaches a method of forming a solder coated material wherein a thin plating of Ni applied by electroplating after which a thicker layer of solder is applied by

wave soldering (col 4 lines 40-45). The plated layer is from 0.5 to 3 microns thick (col 4 lines 53-57 and figure 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conventional method of electroplating to form the thin layer (Sherry, col 1 lines 34-36) while forming the solder by wave soldering and thereby form uniform layers is a reliable and cost-efficient manner (Sherry, col 4 lines 13-18).

11. Claims 24, 31, 33, 35, 36, 38 and 41-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over McAndrew (USPN 6095404) in view of Bartley et al. (USPN 6084775).

McAndrew teaches a method of forming a solder coated material comprising the steps of electroplating a layer of material having excellent solderability such as Ni or Au containing layers having a thickness of 1.27 to 5.5 microns (50 microinches to 220 microinches, col 2 lines 1-15) on a substrate comprising Fe-Ni (col 4 lines 53-59) and then passing the difficult to solder material through molten solder to form a dip solder plating layer having a thickness of about 13 microns (500 microinches) (col 4 lines 20-32) by wave soldering (col 4 line 35). The solderable material may be a Sn-Ag alloy (col 2 lines 30-38). However, there is no disclosure of the substrate as a lead frame, shield or lid.

Bartley teaches a method of soldering a shield (heat sink) module, lid or lead frame (col 1 lines 10-32) by plating a metal having excellent solderability such as Ni or

Au over which is a hot dip plating layer of solder between 1 and 150 microns applied by wave soldering (col 4 lines 5-40).

It would have been obvious to one of ordinary skill in the art at the time of the invention that the substrate can be any type of solderable electronic component or package and that the method of soldering would be the same (McAndrew, col 1 lines 1-27) for lead frames, lids and shield (heat sink) modules which are known components used in the manufacture and assembly of electronics packages (McAndrew, col 2 lines 64-67).

12. Claims 32 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohno (USPN 4666078) in view of Potega (USPN 6152597).

Ohno teaches a method of forming a solder coated material comprising the steps of electroplating a layer of material having excellent solderability such as Ni or Cu (col 2 lines 5-23 having a thickness of 5 microns (col 4 lines 29-37) on a substrate and then passing the difficult to solder material through molten solder (bath) to form a dip solder plating layer having a thickness between 0.1 and 300 microns (col 4 lines 38-63 and col 5 lines 20-61). However, there is no disclosure of the substrate as a lead frame, shield or lid.

Potega teaches a battery cell (col 6 lines 36-46) wherein terminals (electrodes/contacts) are plated with materials having excellent solderability such as Cu (col 6 line 66 – col 7 line 2 and col 23 lines 22-41). Metal platings are typically 1-2

microns thick (col 14 lines 30-41). Parts are joined by wave soldering (col 34 lines 37-48).

It would have been obvious to one of ordinary skill in the art at the time of the invention that the structure of the LCD is similar to the structure of a battery and the methods are forming both are similar. Both comprise plating of terminals to be coated with solder (Ohno, col 1 lines 9-14) and comprise cell structures which are typically sealed (Ohno, col 3 lines 59-65) and driven by current and voltage (Ohno, col 1 lines 14-17 and lines 23-35).

13. Claims 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geschwind (USPN 4331258) in view of Sugihara et al. (US 20010052643 A1).

Geschwind teaches a method of bonding a lid to a package or lead frame (col 2 lines 53-64 and col 3 lines 1-12) comprising the steps of electroplating a layer of material having excellent solderability (gold or nickel) on a substrate comprising Fe-Ni (col 1 lines 25-32 and col 4 lines 12-27) wherein the plated layer is 1.2 to 2.5 microns and the solder layer is 50 microns (2 mils, col 2 lines 35-52). The molten solder is coated by dipping (col 4 lines 32-66). Although the lid is made of a material comprising a sheet to be stamped (col 4 lines 6-12), there is no disclosure of a punching or stamping step after plating.

Sugihara teaches an electronic package which comprises a portion to be soldered comprising an Fe-Ni substrate (paragraphs 50, 64 and 65) which is plated with multiple layers at least one of which is Sn-Ag solder (paragraphs 52 and 62). Plated

layers are applied by electroplating or hot dipping (paragraphs 72-73). The substrate is punched (stamped, coined) after plating (paragraphs 51, 65 and 71).

It would have been obvious to one of ordinary skill in the art at the time of the invention to punch the material after plating to form the lid into the required shape in a simple and cost-effective manner (Geschwind, col 4 lines 1-12) and thereby hermetically seal the semiconductor package (Geschwind, col 1 lines 7-25).

***Response to Arguments***

14. Applicant's arguments with respect to claims 19, 23, 26, 30, 32, 33, 35, 37, 38 and 40 have been considered but are moot in view of the new ground(s) of rejection.

15. Regarding applicant's argument that Geschwind does not teach electroplating or hot dip coating see column 4 lines 55-66 which teach a plating layer particularly an electroplated layer (col 4 line 60) and dip coating in a solder bath (col 4 lines 58-60). However, it is noted that the structures and portions of claims 16 and 20 may comprise a plated layer and solder layer applied by any means which will result in the same structure. The picture frame is taught as a lid for covering a semiconductor package (col 2 lines 20-24). Although Kovar and Alloy 42 are disclosed as suitable but having poor environmental resistance (col 1 lines 25-32), the materials are coated with a plating of about 1 micron upon which is deposited about 50 microns of solder (col 2 lines 48-52) and tested (Table 1, col 3 lines 45-63). Stainless steel is one of the first 8

materials which contains Fe and Ni and is potentially acceptable as a lid material (col 4 lines 13-19). Invar and Kovar are known, conventional lid materials.

Therefore the 102 rejection of claims 16-18, 20-22, 24, 25, 27, 28, 31, 34, 36, 39, 41 and 42 as anticipated by Geschwind stands and now includes claims 44, 46 and 48.

16. Regarding applicant's argument that Nagashima does not teach electroplating or hot dip coating, it is noted that the solder portion structures do not require a particular method to produce the same structure. The reference teaches a plated layer of gold on a substrate comprising Fe-Ni (Kovar) (col 5 lines 1-6 and col 4 lines 16-33) wherein the plating thickness is 0.5 to 5 microns (col 2 lines 15-47 and col 3 lines 3-27). A solder deposit is placed on the plated layer having a thickness of about 50 microns (col 4 lines 17-20) thereby forming the portion to be soldered. The method may be used to join a lid of a packaged part, lead (col 4 lines 16-33) or a connector (col 2 lines 5-14) and may be performed in an inert atmosphere (col 4 lines 5-19).

Therefore the 102 rejection of claims 16-18, 20-22, 24, 31 and 34 as anticipated by Nagashima stands and now includes new claim 44.

***Conclusion***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Majima et al. (USPN 5541447, claimed structure, thicknesses, lead frame), Land (USPN 4119770, battery, plated layer, solder), Lake (USPN 6030721, battery, plated layers), Ito et al. (USPN 5198964, method and structure,

qualitative thickness), Andricacos et al. (USPN 6224690 B1, plated thickness, Fe-Ni substrate, Sn-Ag solder), Do-Thoi et al. (USPN 5156322, method and structure), Tsuji et al. (USPN 5521432, method and structure), Schreiner et al. (USPN 3774427, sonic wave, shield, lid, lead frame), Kato (USPN 5232562, method without solder thickness), Murata et al. (JPN 02-270990), Sato (JPN 09-293958), Obata (JPN 10-102283) and Jin et al. (USPN 6250984 B1).

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne Edmondson whose telephone number is (703) 306-5699. The examiner can normally be reached on M-F from 7-4 with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Dunn can be reached on (703) 308-3318. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-7718 for regular communications and (703) 305-7115 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0651.

Lynne Edmondson
Examiner
Art Unit 1725

4/16/03

LRE
April 16, 2003